REMARKS

Claims 1-22 are pending in the current application. Claims 1-5, 14-20 stand rejected. Claims 21 and 22 are new with this amendment. Claims 6-13 are objected to as being dependent upon a rejected base claim. The Examiner has indicated that claims 6-13 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 6-13 have been rewritten in independent form, and are now in condition for allowance.

35 U.S.C. §112 Rejection

Claims 19-20 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to include a test signal structure. The Examiner has indicated that claims 19 and 20 would be allowable if rewritten to overcome this § 112 rejection. Claim 19 has been amended to include a test signal structure, thereby placing claims 19 and 20 in condition for allowance.

35 U.S.C. §102(b) Rejection

Claims 1, 2, 14 and 18 stand rejected under 35 U.S.C. § 102(b) for allegedly being anticipated by U.S. Pat. No. 4,393,491 by Ashlock, et al. ("Ashlock"). Ashlock does not anticipate claim 1, because Ashlock does not disclose "transmitting the test signal to a destination end point in a plurality of packets having mutually variable sizes" as recited in claim 1. Ashlock is silent as to varying the size of the test signal, and only teaches generating "one eight-bit word" at a time. *See* col. 15, lines 32-35. For the above stated reasons, Ashlock does not anticipate claim 1, or any claims dependent thereon.

Ashlock does not anticipate claim 1, because Ashlock does not disclose or suggest "determining whether the irregularities between the modified test signal and the estimated test signal represent packet loss," as recited in claim 1. Ashlock merely discloses a maintenance card 40 that "includes circuitry to detect the presence of a one-kilohertz tone ... and to indicate the presence or absence of such a signal." *See* col. 7, lines 25-28. Thus, Ashlock simply teaches a pass/fail test, in which a circuit passes if the one-kilohertz tone is present. *See* col. 16, lines 27-28. For the reasons stated above, Ashlock does not anticipate claim 1, or any claims dependent thereon.

Ashlock does not anticipate claim 1, because Ashlock does not teach "comparing the modified test signal pattern to an estimated test signal pattern, the estimated pattern determined by a predefined algorithm," as recited in claim 1. As set forth above, the circuit disclosed in Ashlock simply compares the received signal against the original test signal. For the reasons stated above, Ashlock does not anticipate claim 1, or any claims dependent thereon.

Claim 14 is not anticipated by Ashlock, because Ashlock does not disclose or suggest a "test signal including repeating sections of varying size," as recited in claim 14. Ashlock is silent as to varying the size of the test signal, and simply teaches a test signal of one 8-bit word. *See* col. 7, lines 17-24. For the above stated reason, Ashlock does not anticipate claim 14, or any claims dependent thereon.

Ashlock does not anticipate claim 18, because Ashlock does not disclose or suggest a processor configured to "determine if packet loss occurred during transmission of the signal through the packet network," as recited in claim 18. Ashlock merely teaches a display and alarm circuit 214, which indicates the location of the line that the test signal was not detected. *See* col. 16, lines 42-44. Furthermore, Ashock does not teach the step of "report[ing] test signal packet loss statistics," as recited in claim 18. In addition, Ashock does not teach a test signal "having a predefined pattern of variation in average power level," as recited in claim 18. For the above stated reasons, Ashlock does not anticipate claim 18, or any claims dependent thereon.

35 U.S.C. § 103(a) Rejection

Claims 3-5 and 15-17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ashlock (U.S. 4,393,491). Claims 3-5 and 15-17 are patentable over Ashlock at least for the reasons stated above.

The Examiner admits that Ashlock does not disclose "wherein the lengths of the repeating sections are greater than the largest packet size," as recited in claims 3 and 15. However, the Examiner alleges that it would have been obvious to one of ordinary skill in the art to implement a digital word comprising more than eight-bits in order to stress test the system. The suggested combination would render Ashlock unusable for its intended purpose, because the detection circuitry in Ashlock simply would not detect a test signal greater than

eight-bits. Ashlock teaches that the maintenance card 40 "includes circuitry to detect the presence of a one-kilohertz tone or, more accurately, the digital representation thereof, and to indicate the presence or absence of such a signal." *See* col. 7, lines 25-28. If a digital word comprising more than eight-bits were used in the circuitry as described in Ashlock, the signal would not be greater than a one-kilohertz tone and would not be detected. Thus, Ashlock teaches away from the suggested combination because it does not allow for stress testing the system. For the above stated reasons, claims 3, 15, and all claims dependent thereon, are patentable over Ashlock.

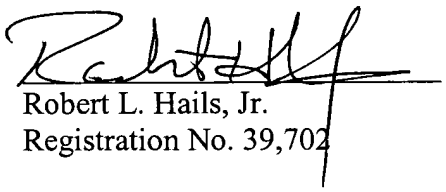
As to claims 5 and 17, the Examiner admits that Ashlock does not disclose a test signal wherein "the section length is equal to four times the segment length," as recited in claims 5 and 17. However, the Examiner alleges that it would have been obvious for one skilled in the art to implement the digital words in Ashlock with 32-bit representation, in order to check for signal loss of long data streams. Ashlock is directed towards testing idle lines to insure that the circuitry for transmitting analog signals and the digital representations thereof are operative. S*ee* col. 2, lines 41-46. Ashlock is silent as to testing for long data streams. Ashlock requires the use of an 8-bit word in order to correspond to eight wires (corresponding to 4 phones having 2 lines each) coupled to the line card 24. *See* col. 4, lines 3-7. Since there is no motivation to use a signal having a section length equal to four times the segment length, claims 5 and 17 are patentable over Ashlock.

CONCLUSION

In view of the foregoing, the Applicants respectfully submit that the application is now in condition for allowance. Should the Examiner have any questions concerning this application, the Examiner is invited to contact the undersigned at the number given below.

Respectfully submitted,
KENYON & KENYON

Dated: January 5, 2005



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